The documentation and process conversion measures necessary to comply with this document shall be completed by 24 March 2004.

INCH-POUND

MIL-PRF-19500/291M
24 February 2004
SUPERSEDING
MIL-PRF-19500/291L
1 May 2003

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, TRANSISTOR, PNP, SILICON, SWITCHING,
TYPES 2N2906A, 2N2906AL, 2N2907A, 2N2907AL, 2N2906AUA,
2N2907AUA, 2N2906AUB, AND 2N2907AUB,
JAN, JANTX, JANTXV, JANJ, JANS, JANHC, AND JANKC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

* The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for PNP, silicon, switching transistors. Five levels of product assurance are provided for each encapsulated device type as specified in MIL-PRF-19500 and two levels of product assurance are provided for each unencapsulated device type.

1.2 Physical dimensions. See figure 1 (similar to a TO-18), figures 2 and 3 (surface mount case outlines UA and UB), and figures 4 and 5 (JANHC and JANKC).

* 1.3 Maximum ratings, unless otherwise specified T_A = +25°C.

I_C	V_{CBO}	V_{EBO}	V_{CEO}	T_J and T_{STG}
mA dc	V dc	V dc	V dc	°C
600	60	5	60	-65 to +200

Types	P_T T_A = +25°C (1) (2)	P_T T_C = +25°C (1) (2)	P_T $T_{SP(IS)}$ = +25°C (1) (2)	P_T $T_{SP(AM)}$ = +25°C (1) (2)	$R_{\theta JA}$ (2) (3)	$R_{\theta JC}$ (2) (3)	$R_{\theta JSP(IS)}$ (2) (3)	$R_{\theta JSP(AM)}$ (2) (3)
	W	W	W	W	°C/W	°C/W	°C/W	°C/W
2N2906A, L,	0.5	1.0 (1)	N/A	N/A	325	150	N/A	N/A
2N2907A, L	0.5	1.0 (1)	N/A	N/A	325	150	N/A	N/A
2N2906AUA,	0.50 (4)	N/A	1.0	1.5	325 (4)	N/A	110	40
2N2907AUA	0.50 (4)	N/A	1.0	1.5	325 (4)		110	40
2N2906AUB,	0.50 (4)	N/A	1.0	N/A	325 (4)	N/A	90	N/A
2N2907AUB	0.50 (4)	N/A	1.0	N/A	325 (4)	N/A	90	N/A

(1) For derating, see figures 6, 7, 8, 9, and 10.
(2) See 3.3 for abbreviations.
(3) For thermal curves, see figures 11, 12, 13, 14, and 15.
(4) For non-thermal conductive PCB or unknown PCB surface mount conditions in free air, substitute figures 7 and 12 for the UA and UB package and use $R_{\theta JA}$.

* Comments, suggestions, or questions on this document should be addressed to Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43216-5000, or emailed to Semiconductor@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http:\\www.dodssp.daps.mil.

1.4 Primary electrical characteristics at T_A = +25°C.

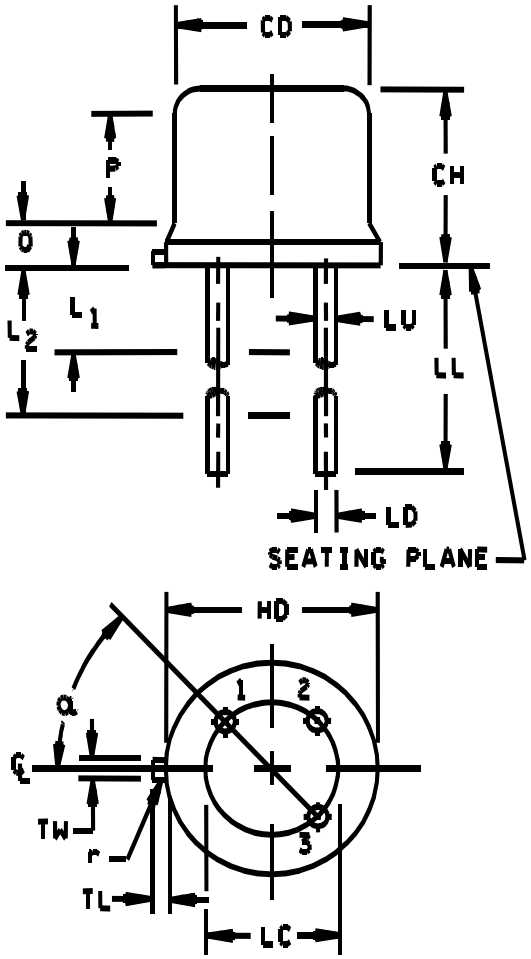
h_{FE} at V_{CE} = 10 V dc										
	h_{FE1} I_C = 0.1 mA dc		h_{FE2} I_C = 1.0 mA dc		h_{FE3} I_C = 10 mA dc		h_{FE4} (1) I_C = 150 mA dc		h_{FE5} (1) I_C = 500 mA dc	
	2N2906A, L, UA,UB	2N2907A, L, UA,UB	2N2906A L, UA,UB	2N2907A L, UA,UB	2N2906A L, UA,UB	2N2907A L, UA,UB	2N2906A L, UA,UB	2N2907A L, UA,UB	2N2906A L, UA,UB	2N2907A L, UA,UB
Min	40	75	40	100	40	100	40	100	40	50
Max			175	450			120	300		

Types	Limit	$\lvert h_{fe} \rvert$ f = 100 MHz V_{CE} = 20 V dc I_C = 20 mA dc	C_{obo} 100 kHz ≤ f ≤ 1 MHz V_{CB} = 10 V dc I_E = 0	Switching (saturated) t_{on} See figure 16	Switching (saturated) t_{off} See figure 17
			pF	ns	Ns
2N2906A, 2N2907A, L, UA, UB	Min	2.0			
	Max		8	45	300

Types	Limits	$V_{CE(sat)1}$ (1) I_C = 150 mA dc I_B = 15 mA dc	$V_{CE(sat)2}$ (1) I_C = 500 mA dc I_B = 50 mA dc	$V_{BE(sat)1}$ (1) I_C = 150 mA dc I_B = 15 mA dc	$V_{BE(sat)2}$ (1) I_C = 500 mA dc I_B = 50 mA dc
		V dc	V dc	V dc	V dc
2N2906A, 2N2907A, L, UA, UB	Min			0.6	
	Max	0.4	1.6	1.3	2.6

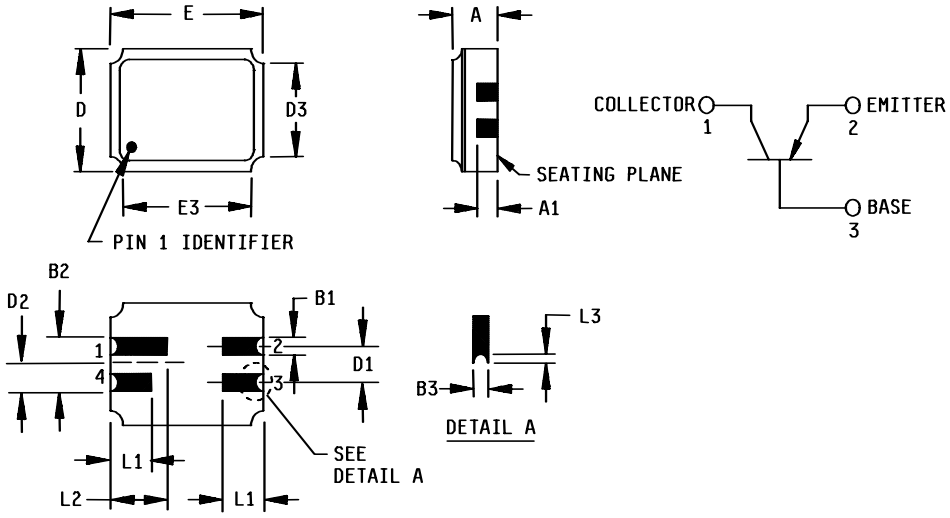
(1) Pulsed see 4.5.1.

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.178	.195	4.52	4.95	
CH	.170	.210	4.32	5.33	
HD	.209	.230	5.31	5.84	
LC	.100 TP		2.54 TP		6
LD	.016	.021	0.41	0.53	7,8
LL	.500	.750	12.70	19.05	7,8,13
LU	.016	.019	0.41	0.48	7,8
L_1		.050		1.27	7,8
L_2	.250		6.35		7,8
P	.100		2.54		
Q		.030		0.76	5
TL	.028	.048	0.71	1.22	3,4
TW	.036	.046	0.91	1.17	3
r		.010		0.25	10
α	45° TP		45° TP		6



NOTES:
1. Dimension are in inches.
2. Millimeters are given for general information only.
3. Beyond r (radius) maximum, TW shall be held for a minimum length of .011 inch (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Body contour optional within zone defined by HD, CD, and Q.
6. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC.
7. Dimension LU applies between L_1 and L_2. Dimension LD applies between L_2 and LL minimum. Diameter is uncontrolled in L_1 and beyond LL minimum.
8. All three leads.
9. The collector shall be internally connected to the case.
10. Dimension r (radius) applies to both inside corners of tab.
11. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.
12. Lead 1 = emitter, lead 2 = base, lead 3 = collector.
13. For L suffix devices, dimension LL = 1.5 inches (38.10 mm) min. and 1.75 inches (44.45 mm) max.

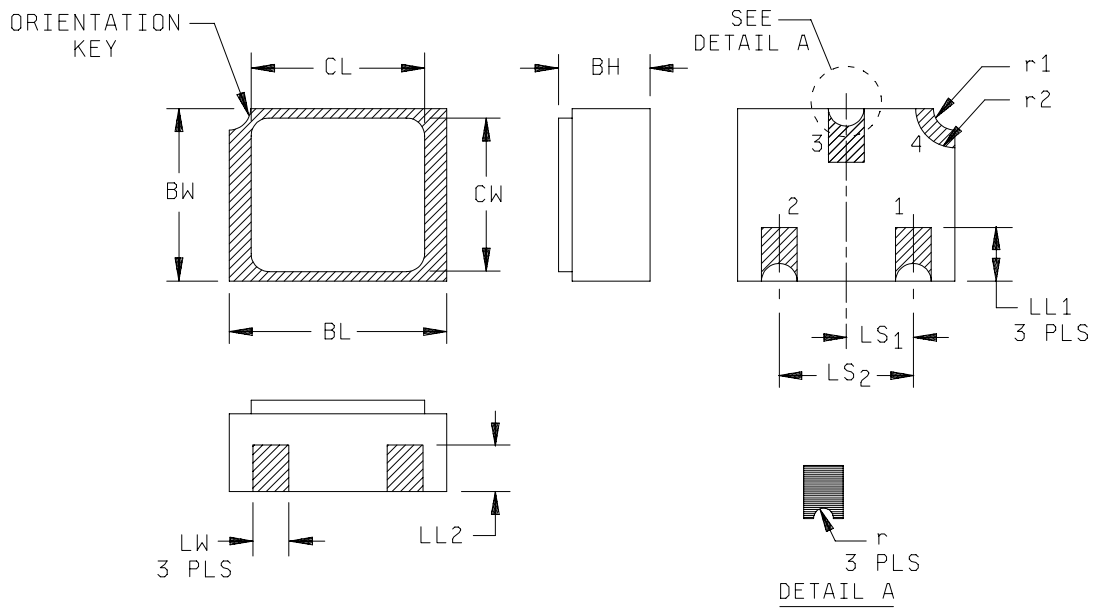
FIGURE 1. Physical dimensions (similar to TO-18).



Ltr	Dimensions				Notes	Ltr	Dimensions				Notes
	Inches		Millimeters				Inches		Millimeter		
	Min	Max	Min	Max			Min	Max	Min	Max	
A	.061	.075	1.55	1.90	3	D_2	.0375 BSC		0.952 BSC		
A_1	.029	.041	0.74	1.04		D_3		.155		3.93	
B_1	.022	.028	0.56	0.71		E	.215	.225	5.46	5.71	
B_2	.075 REF		1.91 REF			E_3		.225		5.71	
B_3	.006	.022	0.15	0.56	5	L_1	.032	.048	0.81	1.22	
D	.145	.155	3.68	3.93		L_2	.072	.088	1.83	2.23	
D_1	.045	.055	1.14	1.39		L_3	.003	.007	0.08	0.18	5

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Dimension "A" controls the overall package thickness. When a window lid is used, dimension "A" must increase by a minimum of .010 inch (0.254 mm) and a maximum of .040 inch (1.020 mm).
4. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
5. Dimensions "B3" minimum and "L3" minimum and the appropriately castellation length define an unobstructed three-dimensional space traversing all of the ceramic layers in which a castellation was designed. (Castellations are required on bottom two layers, optional on top ceramic layer.) Dimension "B3" maximum and "L3" maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dipping.
6. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

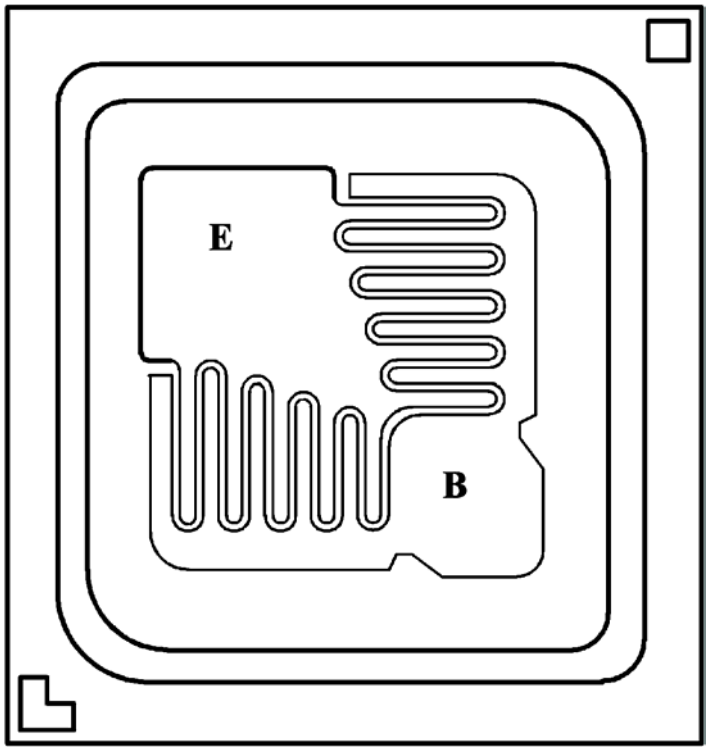
FIGURE 2. Physical dimensions, surface mount (UA version).



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BH	.046	.056	1.17	1.42
BL	.115	.128	2.92	3.25
BW	.085	.108	2.16	2.74
CL		.128		3.25
CW	.085	.108	2.16	2.74
LL1	.022	.038	0.56	0.96
LL2	.017	.035	0.43	0.89
LS1	.035	.039	0.89	.99
LS2	.071	.079	1.81	2.01
LW	.016	.024	0.41	0.61
r1		.012		0.31
r2		.022		0.56

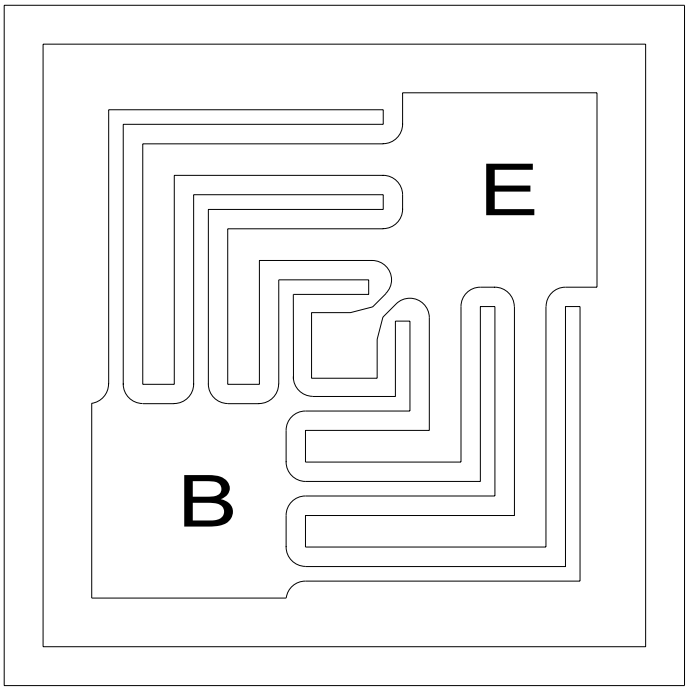
NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Pad 1 = Base, Pad 2 = Emitter, Pad 3 = Collector, Pad 4 = Shielding connected to the lid.
4. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

* FIGURE 3. Physical dimensions, surface mount (UB version).



1. Chip size: 23 x 23 mils ±2 mils (0.584 mm x 0.584 mm).
2. Chip thickness: 10 ±1.5 mils (0.254 mm ±0.038 mm).
3. Top metal: Aluminum 15,000 Å minimum, 18,000 Å nominal.
4. Back metal: A. Al/Ti/Ni/Ag 15kÅ/5kÅ/10kÅ/10kÅ.
   B. Gold 2.5 kÅ minimum, 3.0 kÅ nominal.
   C. Eutectic Die Mount - No metal.
5. Glassivation: SI_3N_4 2kÅ minimum, 2.2k nominal.
6. Backside: Collector.
7. Bonding pad: B = 4.2 x 4.2 mils (0.107 mm x 0.107 mm).
   E = 4.2 x 4.2 mils (0.107 mm x 0.107 mm).

FIGURE 4. JANHC and JANKC (B-version) die dimensions.



1. Die size: 20 x 20 mils square (0.508 mm x 0.508 mm).
2. Die thickness: 8 ± 1.6 mils (0.203 mm ±0.041 mm).
3. Base pad: 4 x 4 mils (0.101 mm x 0.101 mm).
4. Emitter pad: 4 x 4 mils (0.101 mm x 0.101 mm).
5. Back metal: Gold, 6,500 ± 1950 Ang.
6. Top metal: Aluminum, 20,000 ± 2,000 Ang.
7. Back side: Collector.
8. Glassivation: SiO_2, 7,500 ± 1,500 Ang.

FIGURE 5. JANHC and JANKC (D-version) die dimensions.

2. APPLICABLE DOCUMENTS

* 2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

* 2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or www.dodssp.dap.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows.

PCB	Printed circuit board
$R_{\theta JA}$	Thermal resistance junction to ambient.
$R_{\theta JC}$	Thermal resistance junction to case.
$R_{\theta JSP(AM)}$	Thermal resistance junction to solder pads (adhesive mount to PCB).
$R_{\theta JSP(IS)}$	Thermal resistance junction to solder pads (infinite sink mount to PCB).
$T_{SP(AM)}$	Temperature of solder pads (adhesive mount to PCB).
$T_{SP(IS)}$	Temperature of solder pads (infinite sink mount to PCB).
UA, UB	Surface mount case outlines (see figures 2 and 3).

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figures 1, 2, 3, 4, and 5 herein. Epoxy die attach may be used when a moisture monitor plan has been submitted and approved by the qualifying activity.

3.4.1 Lead finish. Lead finish shall be solderable as defined in MIL-PRF-19500. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

3.6 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table I

herein.

3.7 Marking. Marking shall be in accordance with MIL-PRF-19500, except for the UB suffix package. Marking on the UB package shall consist of an abbreviated part number, the date code, and the manufacturer's symbol or logo. The prefixes JAN, JANTX, JANTXV, JANJ and JANS can be abbreviated as J, JX, JV, JJ, and JS respectively. The "2N" prefix and the "AUB" suffix can also be omitted.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500, and as specified herein.

4.2.1 JANJ devices. For JANJ level, 3.3.1 through 3.3.1.3 of MIL-PRF-19500 shall apply, except as modified herein. Supplier imposed requirements, as well as alternate screens, procedures, and/or controls shall be documented in the QM plan and must be submitted to the qualifying activity for approval. When alternate screens, procedures, and/or controls are used in lieu of the JANJ screens herein, equivalency shall be proven and documented in the QM plan. Radiation characterization may be submitted in the QM plan at the option of the manufacturer, however, 3.3.1.1 of MIL-PRF-19500 is not required. Die lot controls and rework requirements shall be in accordance with 3.13 of MIL-PRF-19500 and D.3.13.2.1 for JANS level. Lot formation and conformance inspection requirements for JANJ shall be those used for JANTXV devices as a minimum.

4.2.2 JANJ qualification. For JANJ qualification, 4.4.2.2 herein shall be performed as required by the qualifying activity. A JANS certified supplier may supply JANJ product utilizing the JANJ screening flow in 4.3 herein.

4.2.3 JANHC and JANKC qualification. JANHC and JANKC qualification inspection shall be in accordance with MIL-PRF-19500.

4.2.4 Group E qualification. Group E inspection shall be performed for qualification or requalification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein shall be performed by the first inspection lot of this revision to maintain qualification.

4.3 Screening (JANTX, JANTXV, JANJ, and JANS levels only). Screening shall be in accordance with table IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table IV of MIL-PRF-19500)	Measurement	
	JANS level	JANJ level
1b	Required	Required
2	Optional	Optional
3a 3b 3c	Required Not applicable Required method 3131 of MIL-STD-750 (1)	Required Not applicable Required method 3131 of MIL-STD-750 (1)
4	Required	Optional
5	Required	Required (one pass minimum)
6	Not applicable	Not applicable
7a and 7b	Optional	Optional
8	Required	Not required
9	I_{CBO2}, h_{FE4} read and record	I_{CBO2}, h_{FE4} (Bin and cell)
10	24 hours minimum	24 hours minimum
11	I_{CBO2}; h_{FE4}; ΔI_{CBO2} = 100 percent of initial value or 5 nA dc, whichever is greater. Δh_{FE4} = ±15 percent	I_{CBO2}; h_{FE4}; ΔI_{CBO2} = 100 percent of initial value or 5 nA dc, whichever is greater. Δh_{FE4} = ±15 percent
12	See 4.3.2, 240 hours minimum	See 4.3.2, 160 hours minimum
(2) 13	Subgroups 2 and 3 of table I herein; ΔI_{CBO2} = 100 percent of initial value or 5 nA dc, whichever is greater; Δh_{FE4} = ±15 percent	Subgroups 2 and 3 of table I herein; ΔI_{CBO2} = 100 percent of initial value or 5 nA dc, whichever is greater; Δh_{FE4} = ±15 percent
14a, and 14b	Required	Required
15	Required	Required - attributes data only, film or non-film techniques may be utilized
16	Required	Required

See notes at end of screen table.

4.3 Screening (JANTX, JANTXV, JANJ, and JANS levels only) - Continued.

Screen (see table IV of MIL-PRF-19500)	Measurement
	JANTXV and JANTX level
1b	Required (JANTXV only)
2	Optional
3a	Required
3b	Not applicable
3c	Required method 3131 of MIL-STD-750 (1)
4	Optional
5	Not required
6	Not applicable
7a and 7b	Optional
8	Not required
9	Not applicable
10	24 hours minimum
11	I_{CBO2}, h_{FE4}
12	See 4.3.2, 80 hours minimum
13	Subgroup 2 of table I herein; ΔI_{CBO2} = 100 percent of initial value or 5 nA dc, whichever is greater; Δh_{FE4} = ±15 percent
14a and 14b	Required
15 and 16	Not required

(1) Thermal impedance limits shall not exceed figures 12, 13, 14, 15, and 16.
(2) PDA = 5 percent for screen 13, applies to ΔI_{CBO2}, Δh_{FE4}, I_{CBO2}, and h_{FE4} thermal impedance ($Z_{\theta JX}$) is not required in screen 13.

4.3.1 Screening (JANHC and JANKC). Screening of JANHC and JANKC die shall be in accordance with MIL-PRF-19500, "Discrete Semiconductor Die/Chip Lot Acceptance". Burn-in duration for the JANKC level follows JANS requirements; the JANHC follows JANTX requirements.

* 4.3.2 Power burn-in conditions. Power burn-in conditions are as follows: V_{CB} = 10 - 30 V dc. Power shall be applied to achieve T_J = +135°C minimum using a minimum P_D = 75 percent of P_T maximum, T_A ambient rated as defined in 1.3.

* 4.3.3 Thermal impedance ($Z_{\theta JX}$ measurements). The $Z_{\theta JX}$ measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, and t_{MD} (and V_C where appropriate). The $Z_{\theta JX}$ limit used in screen 3c of 4.3 herein and subgroup 2 of table I shall comply with the thermal impedance graphs in figures 11, 12, 13, 14, and 15 (less than or equal to the curve value at the same t_H time) and/or shall be less than the process determined statistical maximum limit as outlined in method 3131.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein. If alternate screening is being performed in accordance with MIL-PRF-19500, a sample of screened devices shall be submitted to and pass the requirements of subgroups 1 and 2, of table I herein, inspection only (table VIb, group B, subgroup 1 is not required to be performed again if group B has already been satisfied in accordance with 4.4.2).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500, and table I herein. Group A inspection for JANJ shall be in accordance with JANTXV of MIL-PRF-19500 and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table VIa (JANS) of MIL-PRF-19500 and 4.4.2.1. Electrical measurements (end-points) and delta requirements shall be in accordance with table I, subgroup 2 and 4.5.3 herein. See 4.4.2.2 for JAN, JANTX, JANJ and JANTXV group B testing. Electrical measurements (end-points) and delta requirements for JAN, JANTX, JANJ and JANTXV shall be after each step in 4.4.2.2 and shall be in accordance with table I, subgroup 2 and 4.5.3 herein.

* 4.4.2.1 Group B inspection, table VIa (JANS) of MIL-PRF-19500.

Subgroup	Method	Condition
B4	1037	V_{CB} = 10 - 30 V dc.
B5	1027	V_{CB} = 10 V dc; $P_D \geq$ 100 percent of maximum rated P_T (see 1.3). (NOTE: If a failure occurs, resubmission shall be at the test conditions of the original sample.) Option 1: 96 hours minimum sample size in accordance with MIL-PRF-19500, table VIa, adjust T_A or P_D to achieve T_J = +275°C minimum. Option 2: 216 hours minimum, sample size = 45, c = 0; adjusted T_A or P_D to achieve a T_J = +225°C minimum.
B6	3131	$R_{\theta JA}$, $R_{\theta JC}$ only (see 1.3).

* 4.4.2.2 Group B inspection, (JAN, JANTX, JANTXV and JANJ). Separate samples may be used for each step. In the event of a lot failure, the resubmission requirements of MIL-PRF-19500 shall apply. In addition, all catastrophic failures during CI shall be analyzed to the extent possible to identify root cause and corrective action. Whenever a failure is identified as wafer lot and /or wafer processing related, the entire wafer lot and related devices assembled from the wafer lot shall be rejected unless an appropriate determined corrective action to eliminate the failures mode has been implemented and the devices from the wafer lot are screened to eliminate the failure mode.

Step	Method	Condition
1	1039	Steady-state life: Test condition B, 1,000 hours minimum, V_{CB} = 10 dc, power and ambient shall be applied to achieve T_J = +150°C minimum using a minimum of P_D = 75 percent of maximum rated P_T as defined in 1.3. n = 45 devices, c = 0.
2	1039	HTRB: Test condition A, 48 hours minimum. n = 45 devices, c = 0.
3	1032	High-temperature life (non-operating), t = 340 hours, T_A = +200°C. n = 22, c = 0.

4.4.2.3 Group B sample selection. Samples selected from group B inspection shall meet all of the following requirements:

a. For JAN, JANTX, JANTXV and JANJ, samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot. For JANS, samples shall be selected from each inspection lot. See MIL-PRF-19500.

b. Must be chosen from an inspection lot that has been submitted to and passed table I, subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test (subgroups B4 and B5 for JANS, and group B for JAN, JANTX, JANTXV and JANJ) may be pulled prior to the application of final lead finish.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table VII of MIL-PRF-19500, and in 4.4.3.1 (JANS).and 4.4.3.2 (JAN, JANTX, JANTXV and JANJ) herein for group C testing. Electrical measurements (end-points) and delta requirements shall be in accordance with table I, subgroup 2 and 4.5.3 herein.

* 4.4.3.1 Group C inspection, table VII (JANS) of MIL-PRF-19500.

Subgroup	Method	Condition
C2	2036	Test condition E, (not applicable for UA and UB devices).
C6	1027	Test condition B, 1,000 hours, V_{CB} = 10 V dc, power and ambient temperature shall be applied to the device to achieve T_J = +150°C minimum, and minimum power dissipation of 75 percent of max rated P_T (see 1.3 herein); n = 45, c = 0.

4.4.3.2 Group C inspection, table VII (JAN, JANTX, JANTXV and JANJ) of MIL-PRF-19500.

Subgroup	Method	Condition
C2	2036	Test condition E; not applicable for UA and UB devices.
C5	3131	$R_{\theta JA}$ $R_{\theta JC}$ only (see 1.3).
C6		Not applicable.

4.4.3.3 Group C sample selection. Samples for steps in group C shall be chosen at random from any inspection lot containing the intended package type and lead finish procured to the same specification which is submitted to and passes table I tests for conformance inspection. Testing of a subgroup using a single device type enclosed in the intended package type shall be considered as complying with the requirements for that subgroup.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in appendix E, table IX of MIL-PRF-19500 and as specified in table II herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein. Delta measurements shall be in accordance with the applicable steps of 4.5.3.

4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Input capacitance. This test shall be conducted in accordance with method 3240 of MIL-STD-750, except the output capacitor shall be omitted.

4.5.3 Delta requirements. Delta requirements shall be as specified below:

Step	Inspection	MIL-STD-750		Symbol	Limit
		Method	Conditions		
1	Collector-base cutoff current	3036	Bias condition D, V_{CB} = 50 V dc	ΔI_{CB02} (1)	100 percent of initial value or 10 nA dc, whichever is greater.
2	Forward current transfer ratio	3076	V_{CE} = 10 V dc; I_C = 150 mA dc; pulsed see 4.5.1	Δh_{FE4} (1)	$\pm$ 25 percent change from initial reading.

(1) Devices which exceed the table I limits for this test shall not be accepted.

* TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 1 2/						
Visual and mechanical inspection 3/	2071	n = 45 devices, c = 0				
Solderability 3/ 4/	2026	n = 15 leads, c = 0				
Resistance to solvents 3/ 4/ 5/	1022	n = 15 devices, c = 0				
Temp cycling 3/ 4/	1051	Test condition C, 25 cycles. n = 22 devices, c = 0				
Hermetic seal 4/ Fine leak Gross leak	1071	n = 22 devices, c = 0				
Electrical measurements 4/		Table I, subgroup 2				
Bond strength 3/ 4/	2037	Precondition T_A = +250°C at t = 24 hours or T_A = +300°C at t = 2 hours n = 11 wires, c = 0				
Decap internal visual (design verification) 4/	2075	n = 4 devices, c = 0				
Subgroup 2						
* Thermal impedance	3131	See 4.3.3.	$Z_{\theta JX}$			°C/W
Collector to base cutoff current	3036	Bias condition D; V_{CB} = 60 V dc	I_{CBO1}		10	µA dc
Cutoff current, emitter to base	3061	Bias condition D; V_{EB} = 5 V dc	I_{EBO1}		10	µA dc
Breakdown voltage, collector to emitter	3011	Bias condition D; I_C = 10 mA dc; pulsed (see 4.5.1)	$V_{(BR)CEO}$	60		V dc
Collector to emitter cutoff current	3041	Bias condition D; V_{CE} = 50 V dc	I_{CES}		50	nA dc
Collector to base cutoff current	3036	Bias condition D; V_{CB} = 50 V dc	I_{CBO2}		10	nA dc
Emitter to base cutoff current	3061	Bias condition D; V_{EB} = 4 V dc	I_{EBO2}		50	nA dc
Forward-current transfer ratio	3076	V_{CE} = 10 V dc; I_C = 0.1 mA dc	h_{FE1}			
2N2906A, L, UA, UB				40		
2N2907A, L, UA, UB				75		

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 2 - Continued						
Forward-current transfer ratio	3076	V_{CE} = 10 V dc; I_C = 1.0 mA dc	h_{FE2}			
2N2906A, L, UA, UB				40	175	
2N2907A, L, UA, UB				100	450	
Forward-current transfer ratio	3076	V_{CE} = 10 V dc; I_C = 10 mA dc	h_{FE3}			
2N2906A, L, UA, UB				40		
2N2907A, L, UA, UB				100		
Forward-current transfer ratio	3076	V_{CE} = 10 V dc; I_C = 150 mA dc; pulsed (see 4.5.1)	h_{FE4}			
2N2906A, L, UA, UB				40	120	
2N2907A, L, UA, UB				100	300	
Forward-current transfer ratio	3076	V_{CE} = 10 V dc; I_C = 500 mA dc; pulsed (see 4.5.1)	h_{FE5}			
2N2906A, L, UA, UB				40		
2N2907A, L, UA, UB				50		
Collector-emitter saturation voltage	3071	I_C = 150 mA dc; I_B = 15 mA dc, pulsed (see 4.5.1)	$V_{CE(sat)1}$		0.4	V dc
Collector-emitter saturation voltage	3071	I_C = 500 mA dc; I_B = 50 mA dc; pulsed (see 4.5.1)	$V_{CE(sat)2}$		1.6	V dc
Base-emitter saturation voltage	3066	Test condition A; I_C = 150 mA dc; I_B = 15 mA dc; pulsed (see 4.5.1)	$V_{BE(sat)1}$	0.6	1.3	V dc
Base-emitter saturation voltage	3066	Test condition A; I_C = 500 mA dc; I_B = 50 mA dc; pulsed (see 4.5.1)	$V_{BE(sat)2}$		2.6	
Subgroup 3						
High temperature operation		T_A = +150°C				
Collector to base cutoff current	3036	Bias condition D; V_{CB} = 50 V dc	I_{CBO3}		10	µA dc
Low temperature operation		T_A = -55°C				
Forward-current transfer ratio	3076	V_{CE} = 10 V dc; I_C = 10 mA dc	h_{FE6}			
2N2906A, L, UA, UB				20		
2N2907A, L, UA, UB				50		

See footnotes at end of table.

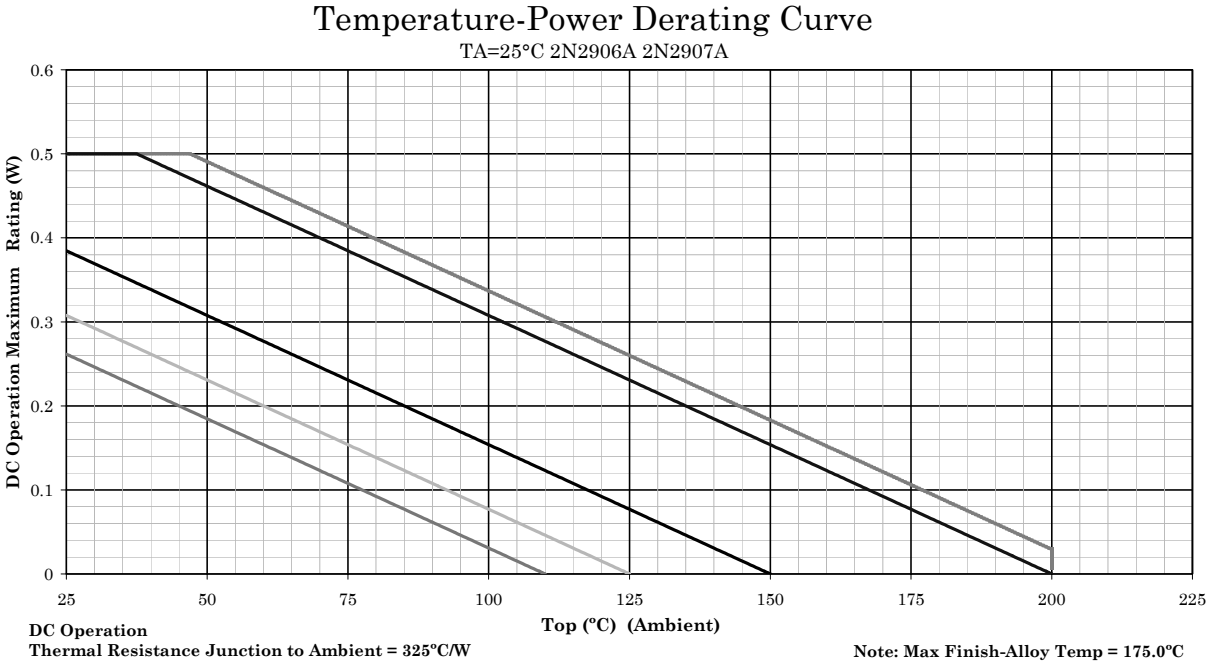
TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 4						
Small-signal short-circuit forward current transfer ratio 2N2906A, L, UA, UB 2N2907A, L, UA, UB	3206	V_{CE} = 10 V dc; I_C = 1 mA dc; f = 1 kHz	h_{fe}	 40 100		
Magnitude of small- signal short- circuit forward current transfer ratio	3306	V_{CE} = 20 V dc; I_C = 20 mA dc; f = 100 MHz	$\|h_{fe}\|$	2.0		
Open circuit output capacitance	3236	V_{CB} = 10 V dc; I_E = 0; 100 kHz ≤ f ≤ 1 MHz	C_{obo}		8	pF
Input capacitance (output open- circuited)	3240	V_{EB} = 2.0 V dc; I_C = 0; 100 kHz ≤ f ≤ 1 MHz	C_{ibo}		30	pF
Saturated turn-on time		(See figure 16)	t_{on}		45	ns
Saturated turn-off time		(See figure 17)	t_{off}		300	ns
Subgroups 5, 6, and 7						
Not applicable						

1/ For sampling plan see MIL-PRF-19500.
2/ For resubmission of failed subgroup of table I, double the sample size of the failed test or sequence of tests. A failure in table I, subgroup 1 shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.
3/ Separate samples may be used.
4/ Not required for JANS devices.
5/ Not required for laser marked devices.

* TABLE II. Group E inspection (all quality levels) - for qualification only.

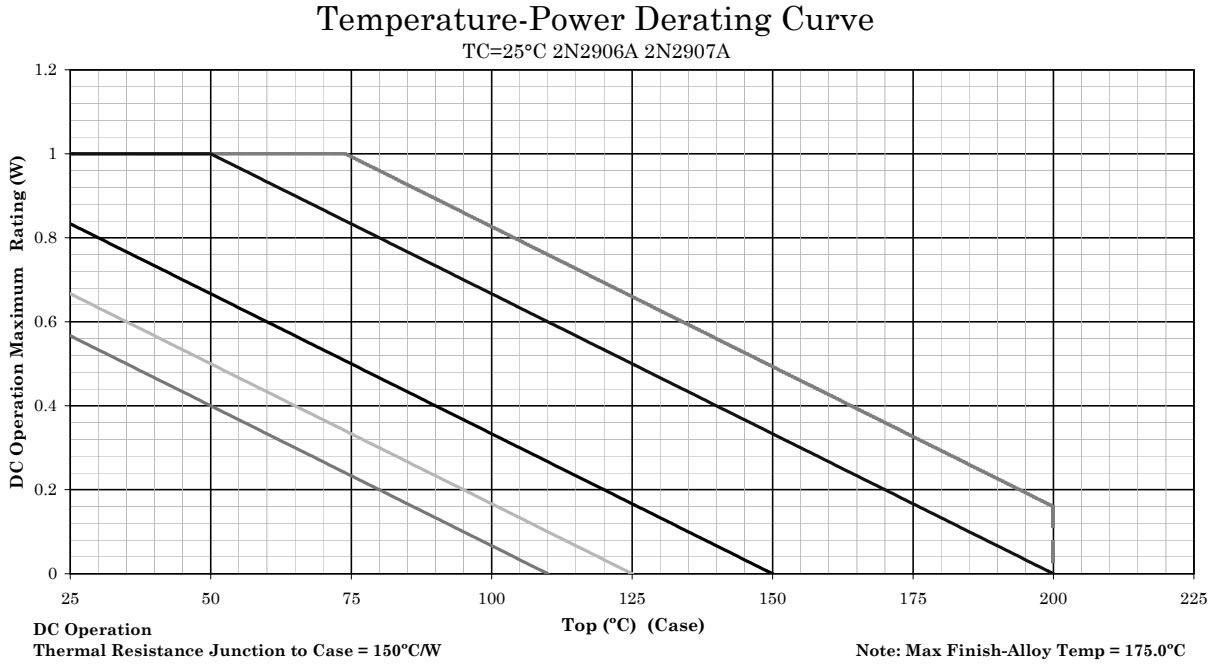
Inspection	MIL-STD-750		Qualification
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles.	
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See table I, subgroup 2 and 4.5.3 herein.	
Subgroup 2			45 devices c = 0
Intermittent life	1037	V_{CB} = 10 V dc, 6,000 cycles.	
Electrical measurements		See table I, subgroup 2 and 4.5.3 herein.	
Subgroup 3			
DPA	2102		3 devices c = 0
Subgroup 4			
Thermal resistance	3131	$R_{\theta JSP(AM)}$, $R_{\theta JSP(IS)}$ only. The following applies for qualification for $R_{\theta JA}$ and $R_{\theta JC}$ can be calculated but shall be measured once in the same package with a similar die size to confirm calculations (can apply to multiple slash sheets).	15 devices c = 0
Thermal impedance curves		Each supplier shall submit their (typical) maximum design thermal impedance curves. In addition, optimal test conditions and $Z_{\theta JX}$ limit shall be provided to the qualifying activity in the qualification report.	Sample size N/A
Subgroup 5			
Not applicable			
Subgroup 6			3 devices c = 0
ESD	1020		
Subgroup 7			45 devices c = 0
Soldering heat	2031	1 cycle	
Electrical measurements		Table I, subgroup 2	
Subgroup 8			45 devices c = 0
Reverse stability	1033	Condition A for devices $\geq$ 400 V, Condition B for devices < 400 V.	



NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified (see 1.3).
3. Derate design curve chosen at $T_J \leq +150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq +125°C$ and +110°C, to show power rating where most users want to limit T_J in their application.

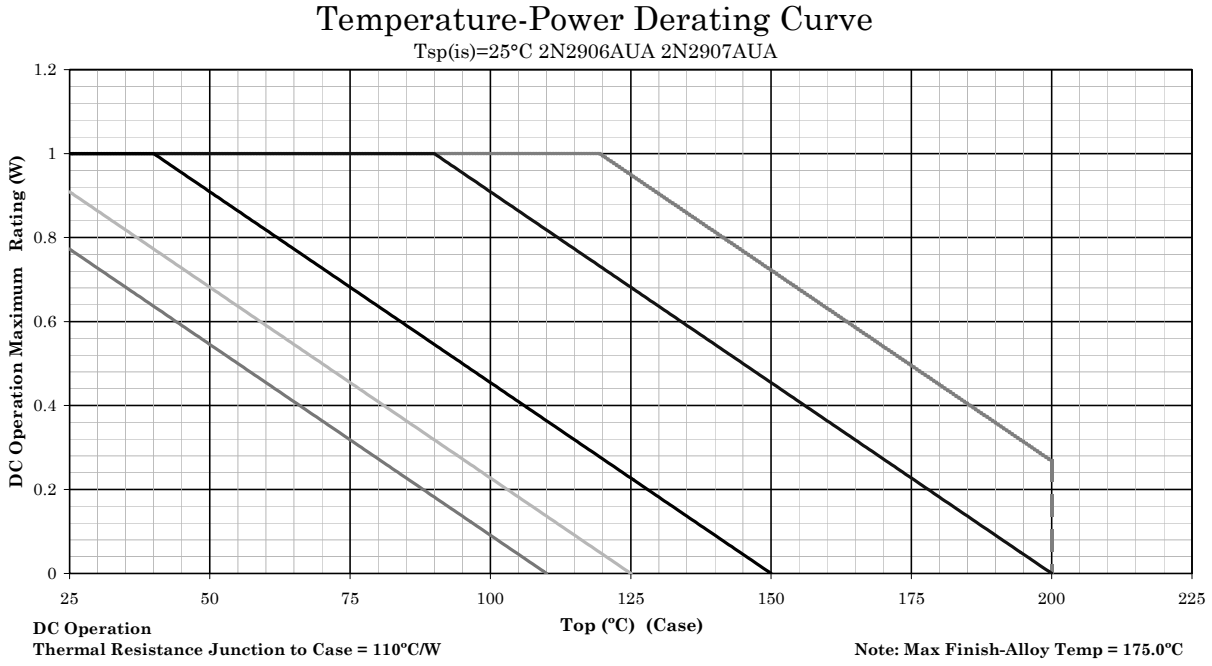
* FIGURE 6. Temperature-power derating for 2N2906A and 2N2907A ($R_{\theta JA}$) leads .125 inch (3.18 mm) PCB (TO-18).



NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified (see 1.3).
3. Derate design curve chosen at $T_J \leq +150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq +125°C$ and +110°C, to show power rating where most users want to limit T_J in their application.

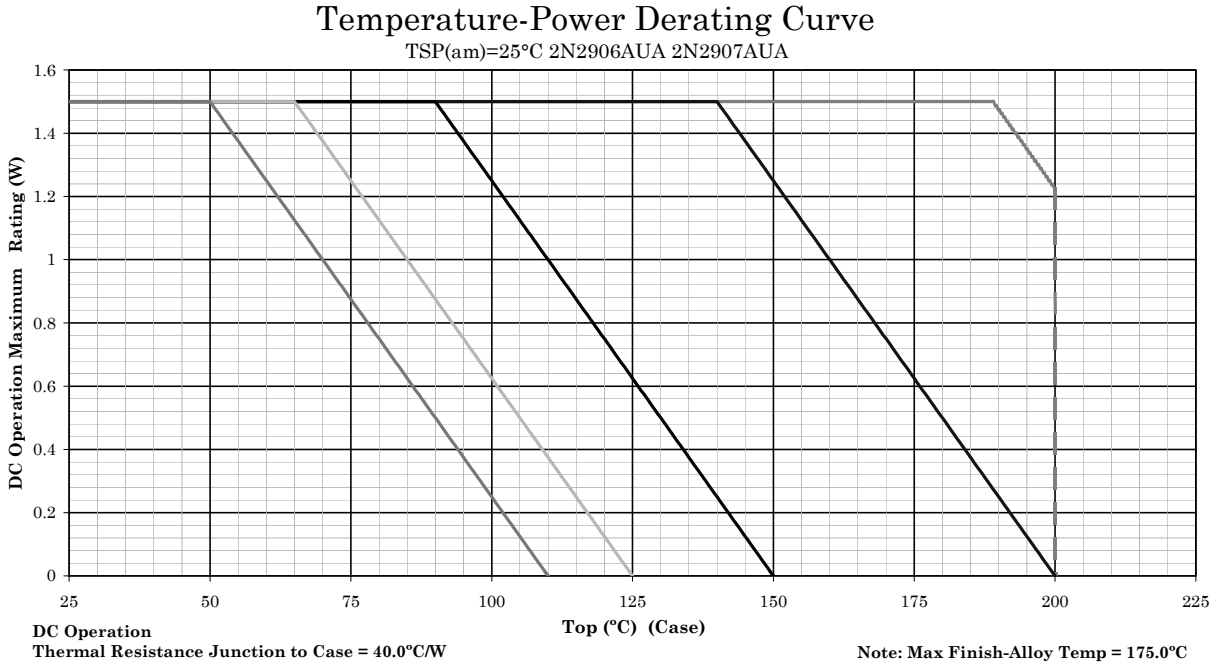
* FIGURE 7. Temperature-power derating for 2N2906A and 2N2907A ($R_{\theta JC}$), base case mount (TO-18).



NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified (see 1.3).
3. Derate design curve chosen at T_J ≤ +150°C, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at T_J ≤ +125°C and +110°C, to show power rating where most users want to limit T_J in their application.

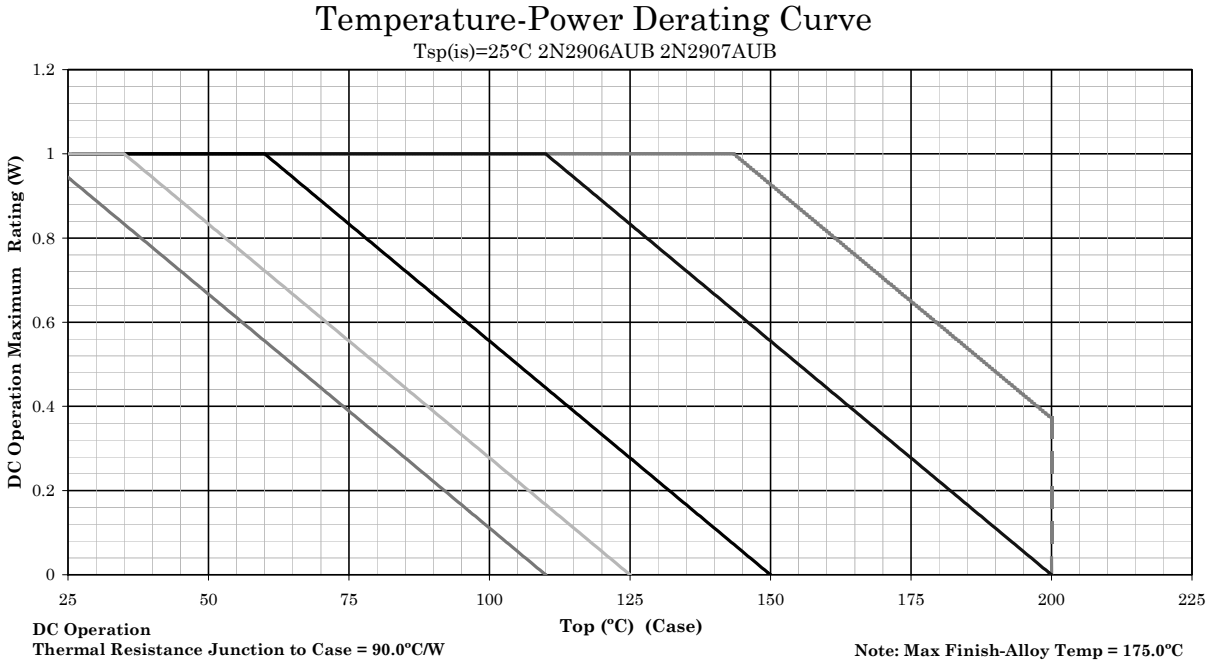
* FIGURE 8. Temperature-power derating for 2N2906AUA and 2N2907AUA ($R_{\theta JSP(IS)}$), infinite sink 4-points.



NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified (see 1.3).
3. Derate design curve chosen at $T_J \leq +150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq +125°C$ and +110°C, to show power rating where most users want to limit T_J in their application.

* FIGURE 9. Temperature-power derating for 2N2906AUA and 2N2907AUA ($R_{\theta JSP(AM)}$) 4-point solder pad (adhesive mount to PCB).



NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified (see 1.3).
3. Derate design curve chosen at T_J ≤ +150°C, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at T_J ≤ +125°C and +110°C, to show power rating where most users want to limit T_J in their application.

* FIGURE 10. Temperature-power derating for 2N2906AUB and 2N2907AUB ($R_{\theta JSP(IS)}$) infinite sink 3-point.

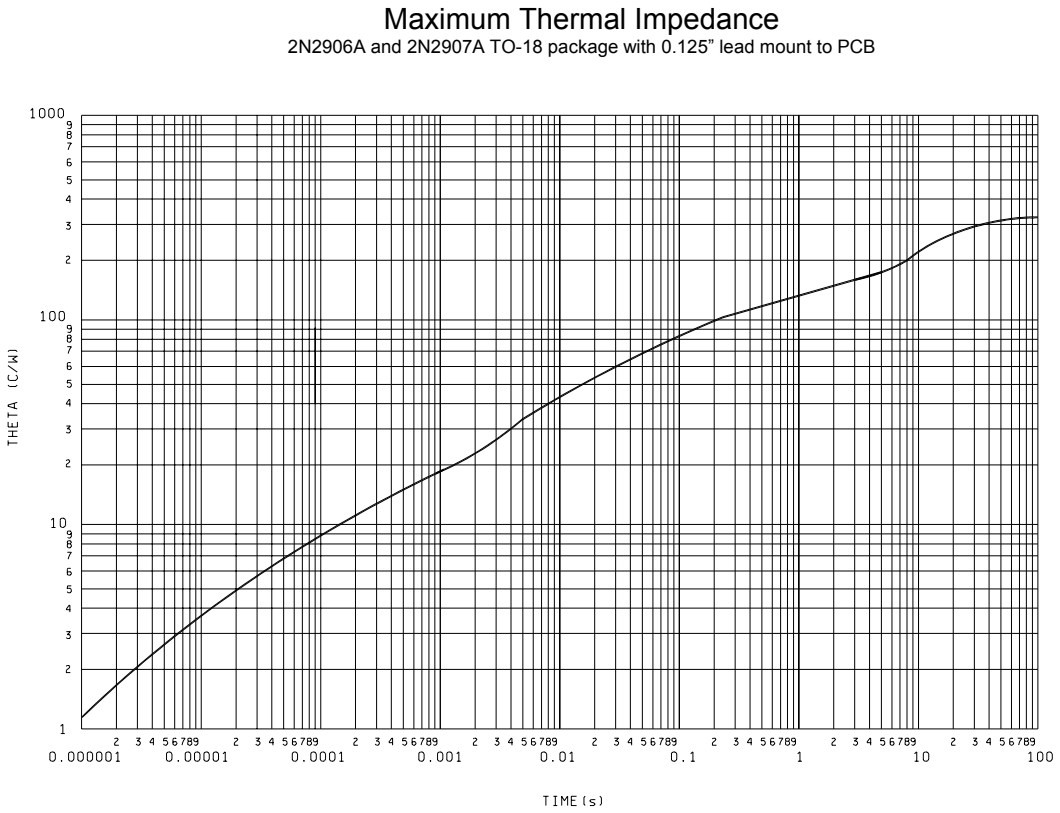


FIGURE 11. Thermal impedance graph ($R_{\theta JA}$) for 2N2906A and 2N2907A (TO-18).

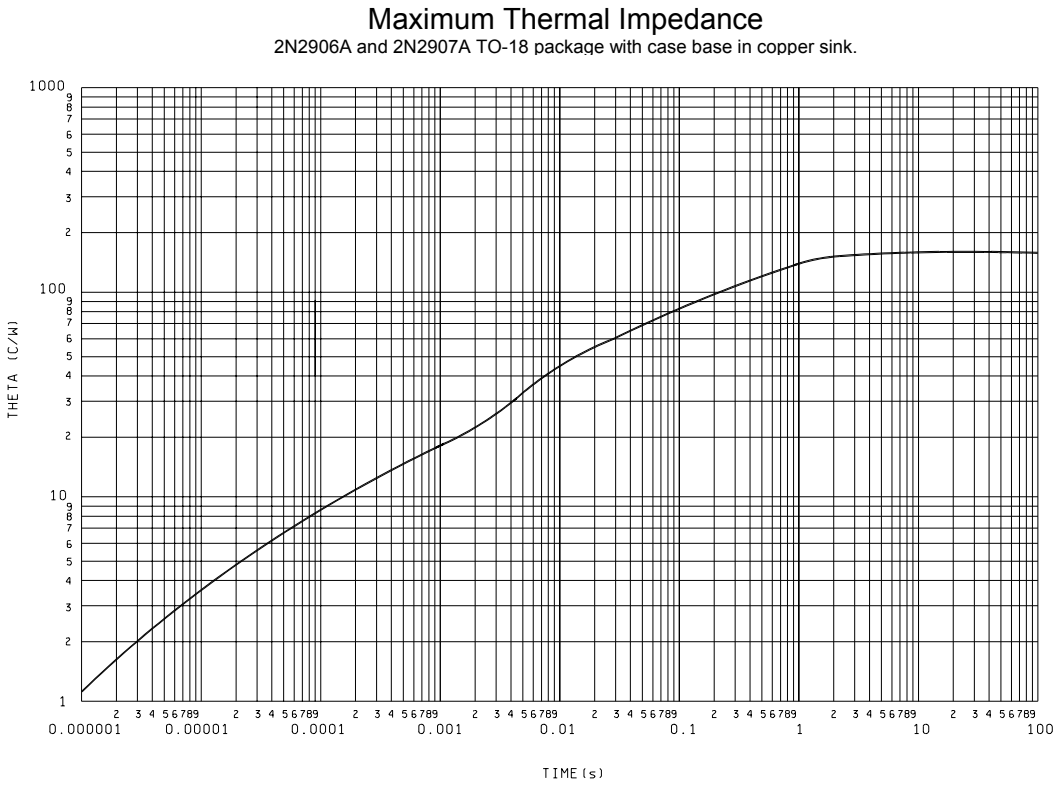


FIGURE 12. Thermal impedance graph ($R_{\theta JC}$) for 2N2906A and 2N2907A (TO-18).

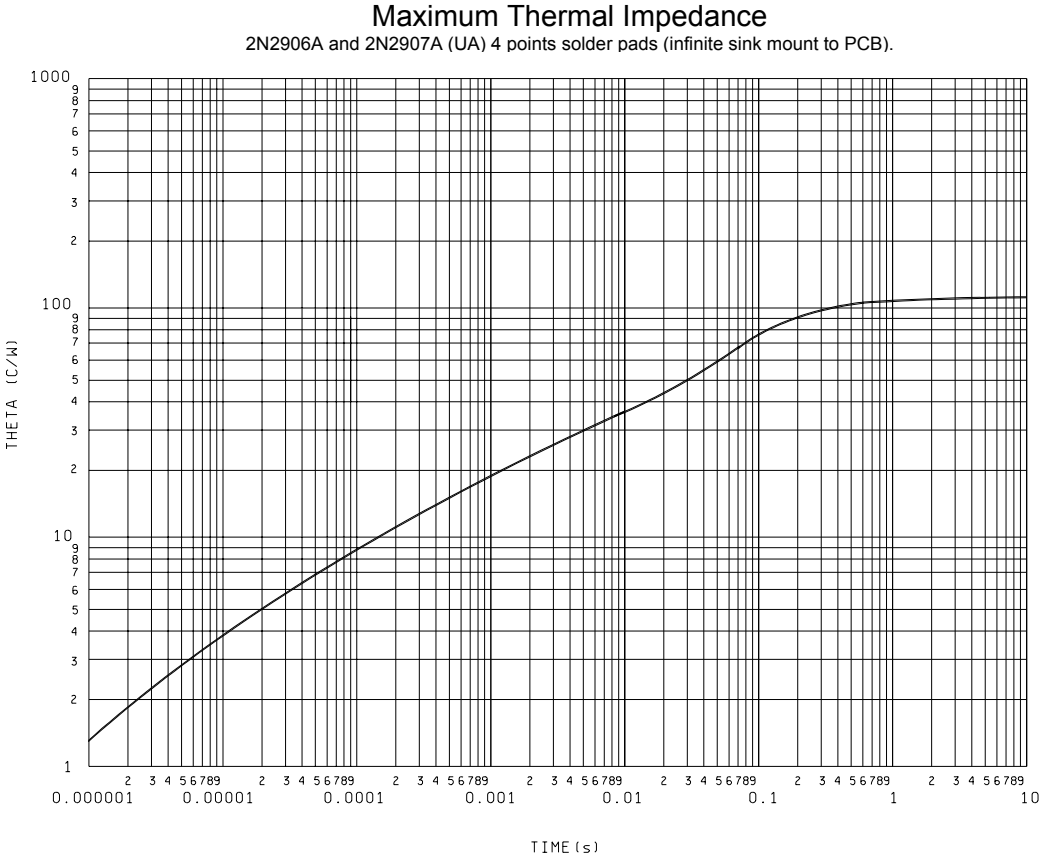


FIGURE 13. Thermal impedance graph ($R_{\theta JSP(IS)}$) for 2N906A and 2N2907A (UA).

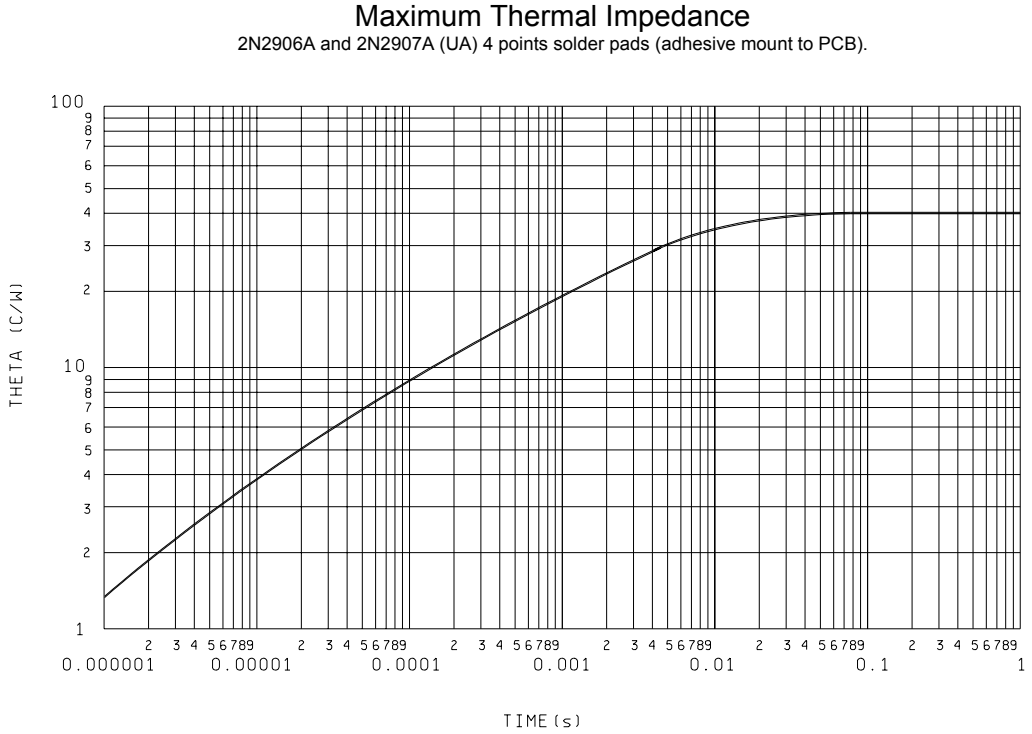


FIGURE 14. Thermal impedance graph ($R_{\theta JSP(AM)}$) for 2N906A and 2N2907A (UA).

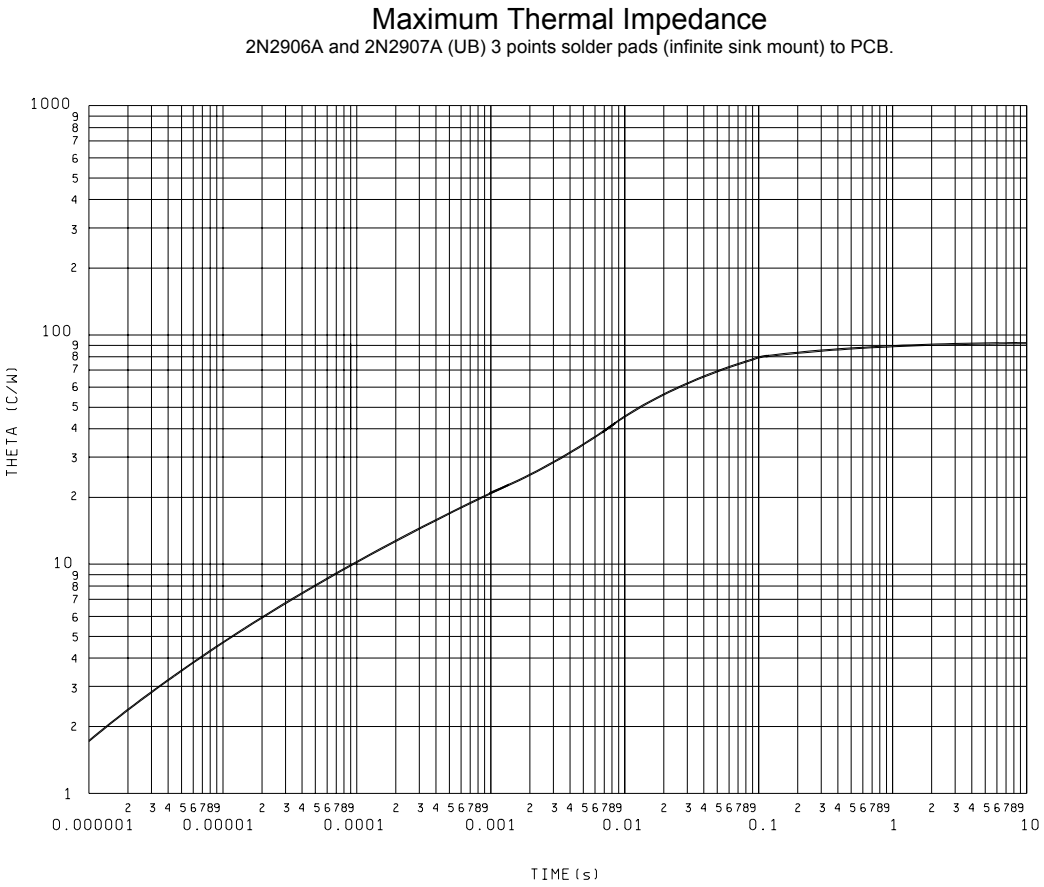
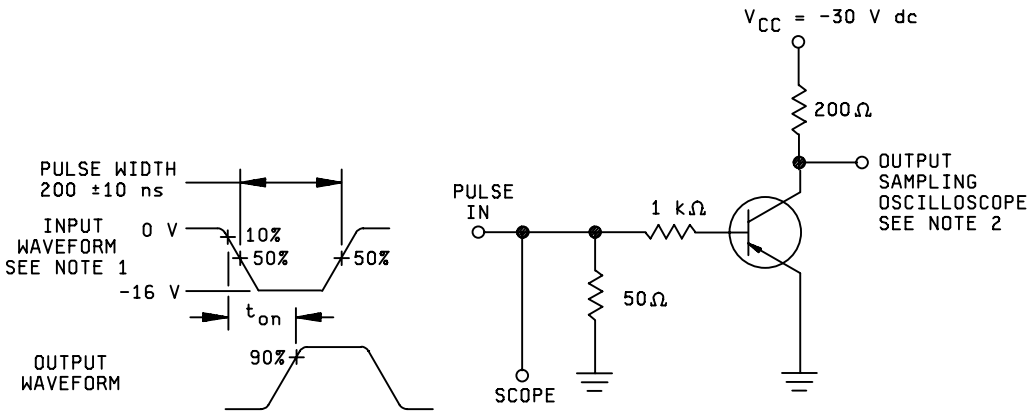


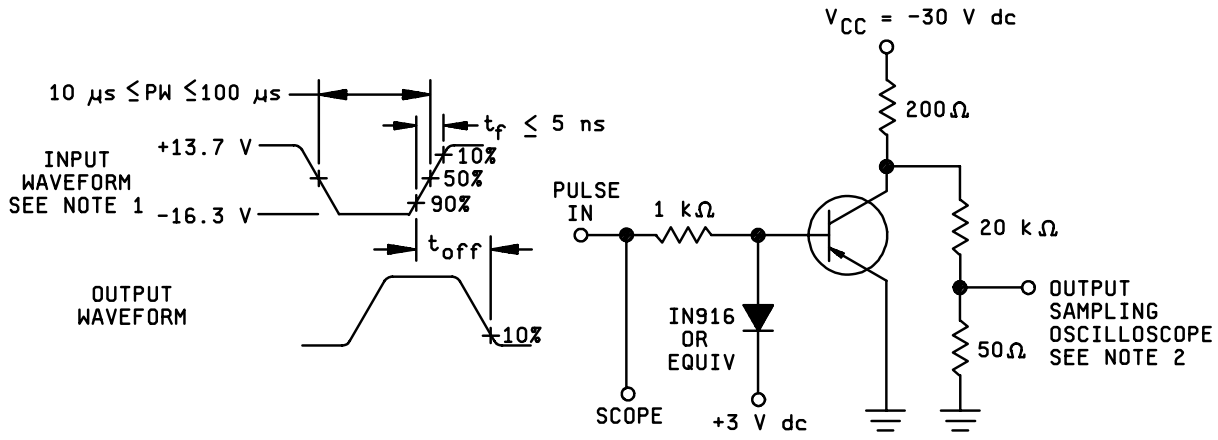
FIGURE 15. Thermal impedance graph ($R_{\theta JSP(IS)}$) for 2N906A and 2N2907A (UB).



NOTES:

1. The rise time (t_r) of the applied pulse shall be ≤ 2.0 ns, duty cycle ≤ 2 percent and the generator source impedance shall be 50 ohms.
2. Sampling oscilloscope: Z_{in} ≥ 100 K ohms, C_{in} ≤ 12 pF, rise time ≤ 5 ns.

FIGURE 16. Saturated turn-on switching time test circuit.



NOTES:

1. The rise time (t_r) of the applied pulse shall be ≤ 2.0 ns, duty cycle ≤ 2 percent and the generator source impedance shall be 50 ohms.
2. Sampling oscilloscope: Z_{in} ≥ 100 K ohms, C_{in} ≤ 12 pF, rise time ≤ 5 ns.

FIGURE 17. Saturated turn-off switching time test circuit.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The notes specified in MIL-PRF-19500 are applicable to this specification.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

d. Product assurance level and type designator.

e. For die acquisition, the letter version must be specified (see figures 4 and 5).

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML-19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC/VQE, P.O. Box 3990, Columbus, OH 43216-5000 or e-mail vqe.chief@dla.mil.

6.4 Supersession information. Devices covered by this specification supersede the manufacturers' and users' Part or Identifying Number (PIN). The term Part or Identifying Number (PIN) is equivalent to the term part number which was previously used in this specification. This information in no way implies that manufacturers' PIN's are suitable as a substitute for the military PIN.

6.5 Suppliers of JANHC and JANKC die. The qualified JANHC and JANKC suppliers with the applicable letter version (example JANHCB2N2907A) will be identified on the QML.

Die ordering information (1) (2)		
PIN	Manufacturer	
	43611	34156
2N2906A 2N2907A	JANHCB2N2906A JANHCB2N2907A	JANHCD2N2906A JANHCD2N2907A

(1) For JANKC level, replace JANHC with JANKC.
(2) JANHCA, JANKCA, JANHCC, and JANKCC versions are obsolete.

6.6 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 11
NASA - NA
DLA - CC

Review activities:
Army - AR, MI, SM
Navy - AS, MC
Air Force - 19, 99

Preparing activity:
DLA - CC

(Project 5961-2873)

* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at http:\\www.dodssp.daps.mil .